Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **Q4**
2. **Q1**
3. **R1**
4. **S1**
5. **ENABLE**
6. **S2**
7. **R2**
8. **VSS**
9. **Q2**
10. **Q3**
11. **R3**
12. **S3**
13. **NC**
14. **S4**
15. **R4**
16. **VDD**

**.064”**

**.054”**

**3 2 1 16**

**15**

**14**

**13**

**12**

**11**

**4**

**5**

**6 7 8 9 10**

**MASK**

**REF**

**CD**

**40**

**43B**

**Top Material: Al**

**Backside Material: SiNi**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VDD**

**Mask Ref: CD4043B**

**APPROVED BY: DK DIE SIZE .054” X .064” DATE: 7/22/21**

**MFG: TIH THICKNESS .025” P/N: CD4043BH**

**DG 10.1.2**

#### Rev B, 7/19/02